

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:

Douglas T. Grider

Docket No:

TI-31118

Serial No:

09/967,044

Conf. No:

4815

Examiner:

Fetsum Abraham

Art Unit:

2826

Filed:

09/28/2001

For:

METHOD FOR TRANSISTOR GATE DIELECTRIC LAYER WITH UNIFORM NITROG

CONCENTRATION

ELECTIO

Assistant Commissioner for Patents Washington, DC 20231

MAILING CERTIFICATE UNDER 37 C.F.R. § 1.8(a) I hereby certify that the above correspondence is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, DC 20231 on 9-19-02

Dear Sir:

This election is offered in response to the Examiner's restriction requirement mailed August 30, 2002.

Applicant hereby elects to pursue Group II of Claims 1-10, drawn to process of making a device, without traversing the Examiner's restriction requirement.

Sespectfully submitted,

Peter K. McLarty Agent for Applicant Reg. No. 44,923

Texas Instruments Incorporated P.O. Box 655474, MS 3999 Dallas, TX 75265 (972) 917-4258